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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/665,663 | 09/20/2000 | Shigeyuki Ueda | ROH-026 | 5545 |

23353 7590 05/30/2002

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

| EXAMINER | |
|---|---|
| COLEMAN, WILLIAM D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2823 | |

DATE MAILED: 05/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/665,663 | UEDA, SHIGEYUKI | |
| | Examiner | Art Unit | |
| | W. David Coleman | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed March 12, 2002 have been fully considered but they are not persuasive.

2. Applicant contends that Idaka et al., U.S. Patent 5,587,337, herein known as Idaka fails to teach each and every limitation of Applicant's claim 1, i.e., an external connection pad and to which a wire for electrical connection to an external terminal is connected.

3. In response to Applicant's contention that Idaka fails to teach an external connection pad and to which a wire for electrical connection to an external terminal is connected, the argument is not convincing. Idaka teaches that the bump electrodes are widely used in logic circuits having a large number of signal terminals. It is well known that signal terminals are wired to provide a functional logic circuit. The most well known wiring circuit for logic circuits is the CMOS inverter. Therefore, Applicant's argument is moot.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Idaka et al., U.S. Patent 5,587,337.

Idaka discloses a semiconductor device as claimed. See **FIG. 3**, where Idaka teaches a semiconductor chip, comprising:

a surface protective film **13**, for covering internal wiring **12**;

an external connection pad **14** which is formed by partially exposing internal wiring **12** from the surface protective film **13**; and

a wire connection portion **3** which is formed using a metal material having oxidation resistance (gold) on the external connection pad **14** and to which a wire for electrical connection to an external terminal is connected.

***Claim Rejections - 35 USC § 103***

6. Claims 2, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Idaka et al., U.S. Patent 5,57,337 as applied to claim 1 above, and further in view of Kawakita et al., U.S. Patent 5,734,199.

7. Pertaining to claim 2, Idaka discloses a semiconductor device substantially as claimed as discussed above, however, Idaka fails to teach wherein the semiconductor chip is overlapped with and joined to a surface of another solid device in a state where the surface protective film is opposed to a surface of the solid device. Kawakita teaches a semiconductor device wherein the surface protective film is opposed to a surface of the solid device. See **FIG. 1** of Kawakita, where Kawakita discloses a semiconductor chip **120** (lower device) having a protective layer **115/125** is overlapped with and joined to a surface of another solid device **110** (upper device). In view of Kawakita, it would have been obvious to one of ordinary skill in the art to incorporate the device of Kawakita into the Idaka device because a first functional element is formed with first testing electrodes (Abstract, 1st sentence).

8. Pertaining to claim 3, Idaka fails to teach an internal connection pad which is partially exposed from the surface protective film in a portion different from the external connection pad, and a bump formed in a raised state on the internal connection pad. Kawakita teaches forming an internal connection pad partially exposed from the surface protective film in a portion different from the external connection pad. See **FIG. 1** of Kawakita, where internal connection pads **113** are located in a different portion than the external connection pads **124**. In view of Kawakita it would have been obvious to incorporate the location of the external connection pads in a different portion of the surface protection film of Idaka so that the semiconductor device can be tested using test electrodes (see Abstract).

9. Pertaining to claim 4, Idaka fail to disclose a solid device, which includes another semiconductor chip. Kawakita teaches interfacing another chip on top of a semiconductor chip. In view of Kawakita, it would have been obvious to incorporate another semiconductor chip on top of a semiconductor chip for LSI technology (column 1, lines 1-24).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Idaka et al., U.S. Patent 5,587,337 as applied to claim 1 above, and further in view of Hayashida et al., U.S. Patent 6,060,768.

Idaka discloses a semiconductor device substantially as claimed, however, Idaka fails to teach that the wire connecting portion is composed of the same material as that for the bump (gold). Hayashida teaches a semiconductor device wherein the wire connection portion is the same material as the bump (gold). See column 14, lines 5-8 and column 15, line19 where Hayashida teaches using a bump and wire of the same material. In view of Hayashida, it would have been obvious to one of ordinary skill in the art to incorporate the same oxidation resistance wire to an

oxidation resistance bump in the Idaka device, because it is well known that the connection of similar materials have excellent adhesion characteristics.

10. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakita et al., U.S. Patent 5,734,199 in view of Hayashida et al., U.S. Patent 6,060,768.

Kawakita discloses a semiconductor device substantially as claimed. Kawakita discloses a semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped and joined to a surface of a primary chip (see **FIG. 1** of Kawakita), wherein said primary chip **110** comprises:

a surface protective film **115/125** for covering internal wiring **126**,

an external connection pad **123** formed by partially exposing the internal wiring from the surface protective film **115/125**,

an internal connection pad **113** which is formed by partially exposing internal wiring **124** from said surface protective film **115/125** in a portion different from external connection pad 126,

and a bump is formed in a raised state on the internal connection pad for electrically connecting the primary chip **110** to the secondary chip **120**.

However, Kawakita fails to teach a wire, connecting portion which is formed using a metal material having oxidation resistance on the external connection pad and forming a bump having oxidation resistance for electrically connecting the primary chip to the secondary chip. Hayashida teaches wherein the bump and wire are the same oxidation resistance material. See column 14, lines 5-8 and column 15, line19 where Hayashida teaches using a bump and wire of the same material. In view of Hayashida, it would have been obvious to form a bump and wire

of the same oxidation resistance material in the Kawakita semiconductor device because of it excellent adhesion properties.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakita et al., U.S. Patent 5,734,199 in vie of Hayashida et al., U.S. Patent 6,060,768 as applied to claim 6 and 7 above and further in view of Nakamura, Japanese Abstract 2000-234904.

12. The combined teachings discloses a semiconductor device substantially as claimed. However, the combined teachings fail to disclose a lead frame and a bonding wire, the bonding wire electrically interconnecting the lead frame and the wire connection portion. Nakamura teaches a lead frame and a bonding wire, the bonding wire electrically interconnecting the lead frame and the wire connection portion. In view of Nakamura, it would have been obvious to one of ordinary skill in the art to incorporate a lead frame and a bonding wire, the bonding wire electrically interconnecting the lead frame and the wire connection portion, because it can provide for a chip-on-chip structure (paragraph 0013).

### *Claim Objections*

13. Claims 2 and 4 are objected to because of the following informalities: the term "solid device" should be "solid state device". Appropriate correction is required.

### *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

WDC
May 24, 2002

LONG PHAM
PRIMARY EXAMINER